Claims

1. (Currently amended) A circuit for testing multiple memories, comprising:

two or more BIST controllers within an integrated circuit, wherein the BIST controllers includes a BIST address port for coupling to address ports of the memories and a BIST data port for coupling to data ports on the memories; and

a resume input on the integrated circuit for receiving a signal, the resume input coupled in parallel to the two or more BIST controllers, wherein the two or more BIST controllers are responsive to the signal on the resume input to exit an idle state, and wherein the resume input comprises a single input pin to the integrated circuit and the signal on the resume input to exit the idle state is asserted through a single channel between automated test equipment (ATE) and the integrated circuit.

2. (Original) The circuit of claim 1, wherein the resume input is an external pin on a perimeter of the integrated circuit for receiving an external signal.

3. (Original) The circuit of claim 1, wherein the resume input is an internal input within the integrated circuit.

4. (Previously Presented) The circuit of claim 1, wherein the two or more BIST controllers include synchronization outputs and the further including:

a signal combiner within the integrated circuit coupled to the synchronization outputs of the BIST controllers, the signal combiner having an output that is activated when a desired number of synchronization outputs from the BIST controllers are activated.

5. (Original) The circuit of claim 4, wherein the signal combiner is a logical AND of the synchronization outputs from the BIST controllers.

6. (Original) The circuit of claim 1, wherein the multiple memories are embedded in the integrated circuit, the memories including a plurality of memory words for storing data, an address port used to identify a memory word during a read or write operation of the memory, a data port that receives data to be written to the memory word during a write operation, and an output port to provide the memory word during a read operation.

7. (Original) The circuit of claim 1, wherein the multiple memories are external to the integrated circuit, the memories including a plurality of memory words for storing data, an address port used to identify a memory word during a read or write operation of the memory, a data port that receives data to be written to the memory word during a write operation, and an output port to provide the memory word during a read operation.

8. (Original) The circuit of claim 2, further including automated test equipment coupled to the resume pin for providing the external signal, wherein the automated test equipment controls the two or more BIST controllers by activating the resume pin.

9. (Original) The circuit of claim 1, wherein BIST controllers include a finite state machine.

10. (Original) The circuit of claim 9, wherein the finite state machine includes a synchronous state wherein a synchronous output of the BIST controller is activated with the finite state machine in the synchronous state.

11. (Original) The circuit of claim 10, wherein the synchronous state is user definable.

12. (Original) The circuit of claim 1, wherein the memories are selected from set including one or more of the following: a dynamic RAM, a static RAM, and a ROM.

13. (Currently amended) A circuit for testing multiple memories, comprising:

at least one BIST controller within an integrated circuit, wherein the BIST controller has a synchronization output which is activated when the controller is in an idle state; and

automated test equipment (ATE), wherein the ATE receives the synchronization output through a single channel between the ATE and the integrated circuit.

14. (Original) The circuit of claim 13, wherein the at least one BIST controller comprises multiple BIST controllers.

15. (Original) The circuit of claim 14, further comprising a signal combiner coupled to the synchronization outputs of the multiple BIST controllers, wherein the combiner output is activated when a desired number of the synchronization outputs are activated.

16. (Original) The circuit of claim 14, further comprising a resume input on the integrated circuit for receiving a signal, wherein the resume input is coupled in parallel to the multiple BIST controllers and wherein the multiple BIST controllers are responsive to the signal to exit the idle state when the signal is activated.

17. (Original) The circuit of claim 13, further including a synchronization pin coupled to the synchronization output so that the synchronization output is externally readable.

18. (Original) The circuit of claim 13, wherein the synchronization output is an internal output within the integrated circuit and is readable by logic within the integrated circuit.

19. (Currently amended) A method of testing memory, comprising:

providing one or more BIST controllers, wherein at least one of the BIST controllers is associated with a group of one or more memories;

independently performing a first phase of a memory test on the group of memories associated with the BIST controller; and

upon completion of the first phase of the memory test, asserting a synchronization signal indicating that the group of memories are at a common synchronization state, wherein the synchronization signal is asserted through a single channel to automated test equipment (ATE).

20. (Original) The method of claim 19, wherein the at least one BIST controller includes two or more BIST controllers, and further comprising combining the synchronization signals from the two or more BIST controllers and providing a combined signal indicating the two or more BIST controllers have finished the first phase of the memory test and have entered a second phase of the memory test in which the controllers are idle.

21. (Original) The method of claim 20, further including receiving a resume signal coupled to the two or more BIST controllers in parallel and continuing a third phase of the memory test in response to the resume signal.

22. (Original) The method of claim 20, wherein the second phase occurs in parallel with respect to at least two groups of memories associated with the two or more BIST controllers.

23. (Original) The method of claim 19, wherein the second phase is part of a retention test of one or more of the memories in the group.

24. (Original) The method of claim 19, wherein the controller is a sequential BIST controller, the group of memories associated with the sequential BIST controller comprises multiple memories, and the second phase occurs in parallel with respect to the multiple memories.

25. (Original) The method of claim 24, further comprising at least one test phase which includes reading from the multiple memories and wherein the reading is interleaved sequentially with respect to the multiple memories.

26. (Original) The method of claim 24, wherein the first phase is a write in parallel to the multiple memories or a sequentially interleaved read of the multiple memories.

27. (Original) The method of claim 19, wherein the second phase is part of an IDDQ test of at least one of the memories in the group of memories.

28. (Original) The circuit of claim 19 further comprising additional phases of the memory test wherein at least some of the phases correspond to a checkerboard type pattern or a march type pattern.

29. (Original) The circuit of claim 19 wherein the BIST controller initiates placing itself into the second phase where it remains idle.

30. (Currently amended) A method of testing memories, comprising:

providing at least a first BIST controller within an integrated circuit, the first BIST controller coupled to a first group of one or more memories, wherein the at least a first BIST controller comprises at least an additional second BIST controller that is coupled to a second group of two or more memories;

using the first BIST controller, performing a first phase of a memory test on the first group of memories;

upon completion of the first phase of the memory test in the first BIST controller, entering an idle state, wherein the first BIST controller enters the idle state under its own initiative;

using the second BIST controller, performing a first phase of a memory test on the second group of memories, independent of the first BIST controller;

upon completion of the first phase of the memory test in the second BIST controller, entering an idle state, wherein the second BIST controller enters the idle state under its own initiative;

coupling a resume input on the integrated circuit to the first and second BIST controllers, wherein the resume input comprises a single input pin to the integrated circuit and a signal on the resume input is asserted through a single channel between automated test equipment (ATE) and the integrated circuit; and

in response to activation of the resume input, exiting the idle state in the first and second BIST controllers.

31. (Canceled)

32. (Previously Presented) The method of claim 30, further including coupling the first and second BIST controllers to a combined output, wherein the combined output is activated when the first and second BIST controllers enter the idle state.

33. (Canceled)

34. (Currently amended) A computer readable medium on which is stored a software tool that inserts BIST controllers into circuits that test memory elements, the tool containing instructions for performing the following:

reading a description of a user-defined test algorithm for a BIST controller, wherein the algorithm includes having the BIST controller enter into one or more synchronization states in which the controller enters an idle state, wherein the controller remains in an idle state until activation of a resume input, wherein the resume input comprises a single input pin to an integrated circuit comprising the BIST controller and a signal on the resume input is asserted through a single channel between automated test equipment (ATE) and the integrated circuit;

translating the description into an in-memory representation of the user-defined algorithm;

reading a memory model selected by a user;

associating the in-memory representation of the user-defined algorithm with the selected memory model; and

generating an HDL description of a BIST controller operable to apply the user-defined algorithm to a memory corresponding to the selected memory model.

35. (Previously Presented) The computer readable medium of claim 34 wherein the algorithm description includes one or more programming language key words associated with the synchronization state.

36. (Previously Presented) The computer readable medium of claim 34, further comprising, from the HDL description, fabricating multiple BIST controllers as part of an integrated circuit, wherein the controllers perform synchronization states in parallel.

37. (Previously Presented) The method of claim 30, further including coupling N BIST controllers in parallel with the first and second BIST controllers, wherein the N BIST controllers enter an idle state under their own initiative to synchronize memory testing between the BIST controllers.